[1] What happens during a *read* bus cycle of 8086 microprocessor in each of the following states ?

   a) T1 :   ALE , will activated at T1 only
              DT/R , will activated at T1 – T4
              IO/M , will activated at T1 – T4
              BHE , will activated at   T1- T4

   b) T2 :   DEN , will activated at T2 – T4
              RD , will activated at T2- T4

   c) T3 : wait state will be inserted if it needed , and used to all memory to access data

   d) T4 : all control signal addresses will be deactivated in preparation for the next clock cycle

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[2] What are the operational modes of an Intel 8086 microprocessor and how do they differ?

   Minimum mode and Maximum mode

2.5

[3] Which mode of 8086 is required for the multiprocessor system?
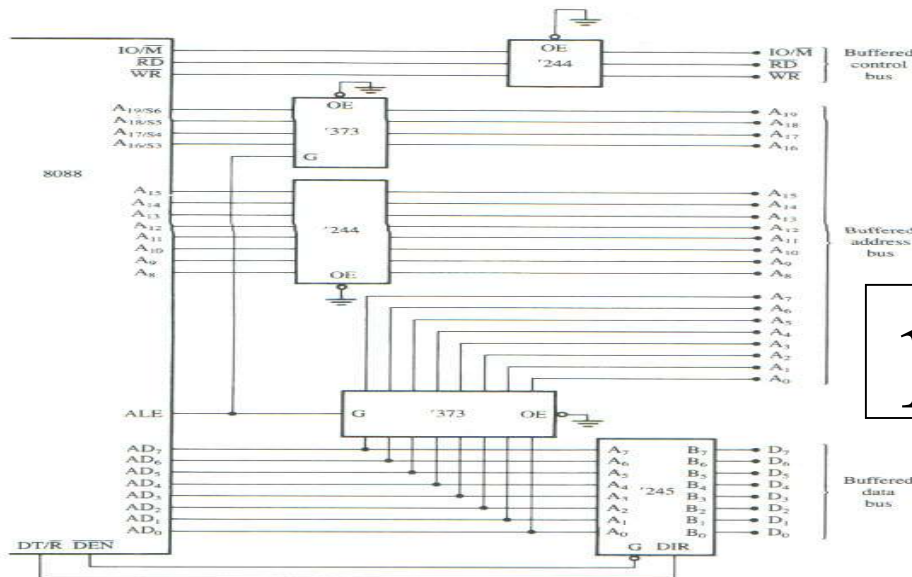
   Maximum mode

2.5

[4] What main function is provided by 8288 bus controller when used with 8086/8088 maximum mode operation?

   it provides a control signal that are not provided at maximum mode such as
     MRDC ,MRTC , AMWC, IORC , IOWC , INTA , DEN

2.5

[5] Draw a block diagram of fully buffered 8086 microprocessor ?

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[6]   a : MOV AH,DS:BYTE PTR[F3C6]   b : MOV CX,DS:WORD PTR[0ABE]
        c : MOV IP,DS: [0001]   d : MOV AX,SS:[000BH]

   find out the information required to complete table below from the above instructions

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ADDRESS	DATA TYPE	BHE (ACTIVE LOW)	A0	BUS CYCLES	DATA LINES USED
even	Byte	1	0	1	D0- D7
even	Word	0	0	1	D0-D15
odd	Word	0 1	1 0	2	D8-D15 D0-D7
odd	Word	0 1	1 0	2	D8-D15 D0-D7

   • Assume all the segment register have an even addresses.

[6]   What   are   the   advantages   of   having   isolated   I/O   over   memory   mapped   I/O?

   - to provide more space for data/codes instead of using it for I/O address space

2.5

[7] List the types of 8086 I/O port numbers?, In addition to show that there are at least two things discriminate between them?

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fixed I/O port   variable I/O port

1- any I/O port less or equal than FFh are fixed port number, any I/O port greater than FFH known as variable port number

2- variable port number must loaded at DX register once we use I/O instruction while fixed we can use it directly with I/O instruction

[8] For 8088 system , draw the timing diagram for the following instruction : Mov AL, [1000] ? ASSUME DS=1000H

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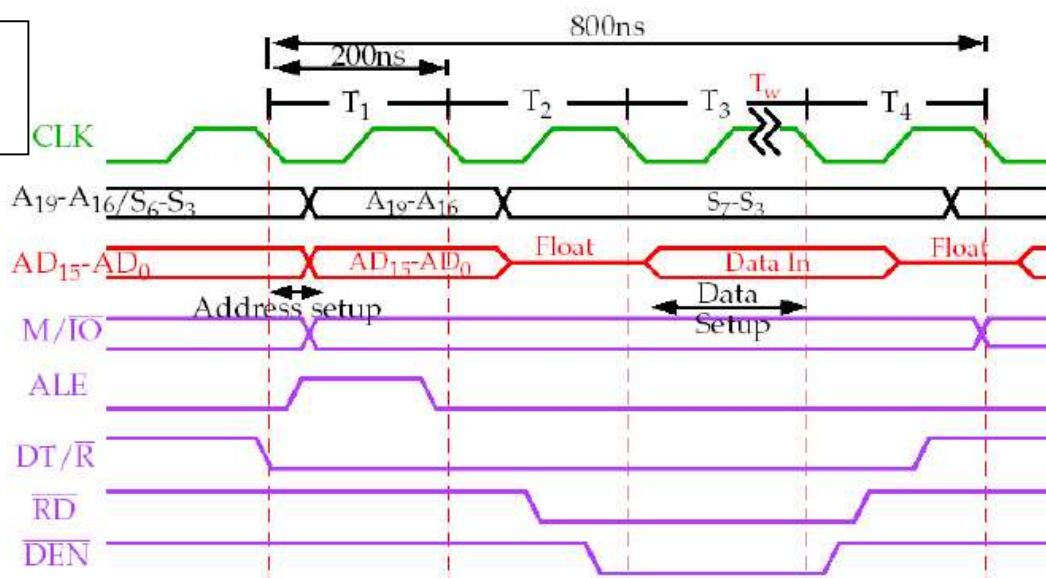
[9] For an 8088 microprocessor, use the NAND-gate technique (only NAND gates and inverters allowed) to map the upper most eighth (1/8) of the memory (ending at FFFFF) into four identical EPROM chips. Find out the size of suitable EPROM chip. Draw the circuit and indicate the start and the end addresses accessible through each EPROM. Use the control signals of microprocessor to access memory.
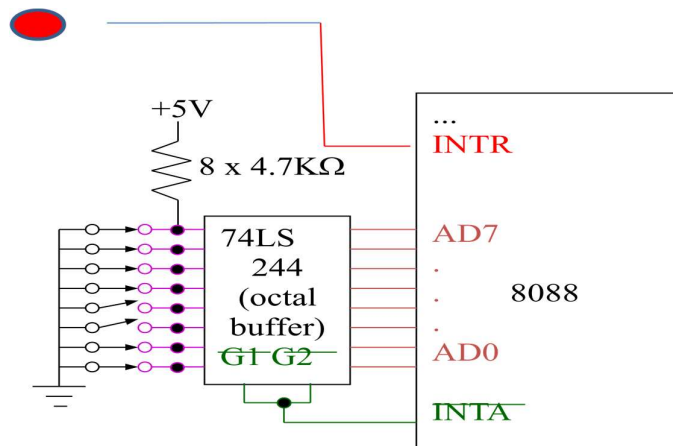
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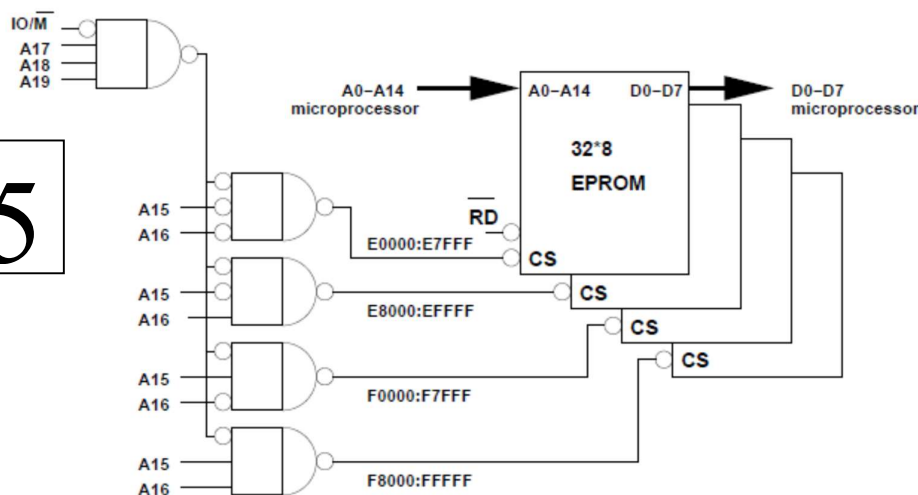
[10] The external interrupt source (INTR) has connected to the output of ground switch. Whenever any person has step over it , INTR will activated.
Write assembly program that count the number of person passing over this switch.

The interrupt vector number provide for the microprocessor as response for the INTA signal is =
00001100 = 0Ch
N= 0Ch   ,   N*4 = 30H

The program:
. model small
. stack 64
. data
. code
        MOV AX, @data
        MOV DS, AX
MOV BX, 0000h
XOR AX, AX
MOV ES, AX
MOV DI, 0030h
MOV ES:[DI], offset XIP
MOV ES:[DI+2], seg YCS
Waiting: JMP waiting

YCS segment
    Assume CS:YCS
      XIP: INC BX
        IRET
 YCS ENDS

END

================================GOOD LUCK =======================================